ABSTRACT OF THE DISCLOSURE

An integrated circuit processor core 4 is provided with an instruction pipeline 20 along which program instructions advance. When an exception condition occurs part way through execution of a particular program instruction, then a prefetch of the exception handling program instruction corresponding to that exception is initiated before the currently executing program instruction has completed. In this way the exception handling program instruction is more rapidly available to start the exception processing. The early prefetch may involve performing a lookup in a cache memory 6 and any necessay linefill upon a miss. In addition, the exception handling program instruction amy also be fed into the instruction pipeline 20 before an instruction boundary is reached.

[Figure 1]